IN THE CLAIMS

Please add new claims 59-63, as set forth below.

The text of all pending claims, along with their current status, is set forth below:

1. (Previously presented) A plurality of generally elliptical capacitive memory elements, each capacitive memory element having a first electrode with an interior portion forming a pair of concentric sidewalls extending perpendicularly from a substrate, the plurality of capacitive memory elements disposed on the substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

2. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

3. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a processor.

4. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises a memory device.

5. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein the substrate comprises an integrated circuit device.

6-7. (Canceled)

8. (Original) The plurality of capacitive memory elements set forth in claim 1 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

9. (Withdrawn) A plurality of capacitive memory elements arranged in a first row and a second row so that an axis through any of the plurality of capacitive memory elements located in the first row does not form an axis of any capacitive memory element in the second row.

10. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the plurality of capacitive memory elements is disposed on a substrate.

11. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is not generally parallel with an edge of the substrate.

12. (Withdrawn) The plurality of capacitive memory elements set forth in claim 11 wherein the axis is not generally perpendicular with an orthogonal of the substrate.

13. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises a processor.

14. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises a memory device.

15. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the substrate comprises an integrated circuit device.

16. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is slanted with respect to the edge of the substrate.

17. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

18. (Withdrawn) The plurality of capacitive memory elements set forth in claim 17, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

19. (Withdrawn) The plurality of capacitive memory elements set forth in claim 9 wherein the axis is a longitudinal axis through one of the capacitive memory elements.

20. (Previously presented) An integrated circuit device, comprising:

a substrate;

a memory array that includes a plurality of memory cells disposed on the substrate, the memory array comprising a plurality of capacitive memory elements, each of the capacitive memory elements being associated with one of

the plurality of memory cells, each capacitive memory element having a first electrode with an interior portion forming a pair of concentric sidewalls extending perpendicularly from the substrate, the plurality of capacitive memory elements being disposed on the substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

21. (Original) The integrated circuit device set forth in claim 20 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

22. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a processor.

23. (Original) The integrated circuit device set forth in claim 20 wherein the substrate comprises a memory device.

24-25. (Canceled)

26. (Original) The integrated circuit device set forth in claim 20 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

27. (Withdrawn) The integrated circuit device set forth in claim 26 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

28. (Withdrawn) The integrated circuit device set forth in claim 24 wherein the substrate comprises a processor.

29. (Withdrawn) The integrated circuit device set forth in claim 24 wherein the substrate comprises a memory device.

30. (Withdrawn) The integrated circuit device set forth in claim 24 wherein each of the plurality of capacitive memory elements is slanted with respect to the edge of the substrate.

31. (Withdrawn) The integrated circuit device set forth in claim 24 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

32. (Withdrawn) The integrated circuit device set forth in claim 31, wherein each of the plurality of capacitive memory elements is generally ellipsoidal.

33. (Withdrawn) The integrated circuit device set forth in claim 24 wherein the axis is a longitudinal axis.

34. (Withdrawn) An electronic device, comprising:

a processor adapted to executed instructions;

a storage device adapted to store instructions to be executed by the processor;

a user input device adapted to receive data for use by the processor from a user;

a display device adapted to produce an image for viewing by a user based on instructions executed by the processor; and

a memory device that receives information stored on the storage device, the memory device comprising:

a substrate; and

a plurality of capacitive memory elements disposed on the substrate so that an axis that runs longitudinally through one of the plurality of capacitive memory elements is not generally parallel with an edge of the substrate.

35. (Withdrawn) The electronic device set forth in claim 34 wherein the axis is not generally perpendicular with an orthogonal edge of the substrate.

36. (Withdrawn) The electronic device set forth in claim 34 wherein each of the plurality of capacitive memory elements is generally oblong in shape.

37-57. (Canceled)

58. (Withdrawn) A plurality of capacitive memory elements disposed on a substrate in a first row and a second row so that an axis through any of the plurality of capacitive memory elements located in the first row does not form an axis of any capacitive memory element in the second row and so that the axis is not generally parallel with an edge of the substrate.

59. (New) A plurality of generally elliptical capacitive memory elements on a surface of a substrate, each capacitive memory element having a first electrode with a generally elliptical outer sidewall and a generally elliptical inner sidewall, wherein the generally elliptical inner sidewall defines a generally right-elliptical-cylindrical volume with a generatrix that is generally perpendicular to the surface of the substrate, the plurality of capacitive memory elements disposed on the substrate along wordlines, wherein at least one of the plurality of capacitive memory elements is oriented so that its major axis is neither generally parallel nor generally perpendicular to the wordlines.

60. (New) The plurality of generally elliptical capacitive memory elements set forth in claim 59, wherein each of the plurality of capacitive memory elements is oriented so that the major axes of each of the plurality of capacitive memory elements are neither generally parallel nor generally perpendicular to the wordlines.

61. (New) The plurality of generally elliptical capacitive memory elements set forth in claim 59, wherein the plurality of capacitive memory elements are disposed on the substrate in an upright-square-lattice arrangement.

62. (New) The plurality of generally elliptical capacitive memory elements set forth in claim 59, wherein the at least one of the plurality of capacitive memory elements is oriented so that its major axis is at a generally 5-degree angle to either the wordlines or a line perpendicular to the wordlines.

63. (New) The plurality of generally elliptical capacitive memory elements set forth in claim 59, wherein the at least one of the plurality of capacitive memory elements is oriented so that its major axis is at a generally 18-degree angle to either the wordlines or a line perpendicular to the wordlines.